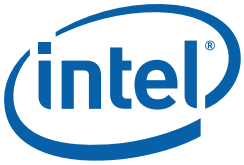

Using 24-bpp LVDS Panels with Intel® Mobile Chipsets for Embedded Applications

White Paper

December 2006

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Revision History

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§

1 Introduction

There is a growing demand from embedded system designs to be able to use 24-bpp LVDS panels with the following Intel mobile graphics chipsets: Intel® 852GM, Intel® 852GME, Intel® 855GME, Intel® 915GM and Intel® 945GM. Unfortunately, the integrated LVDS transmitter in these chipsets only specify support for 18-bpp panels.

This document will examine the various options open to system designers who wish to use 24-bpp panels. It will cover the use of external transmitters and also a workaround to enable the use of the integrated transmitter.

1.1 Terminology

For this document, the following terminology applies

- *Mobile GMCH* refers to the Intel® 82852GM, Intel® 82852GME, Intel® 82855GME, Intel® 82915GM and Intel® 82945GM GMCH
- *852GM* refers to the Intel® 82852GM GMCH
- *852GME* refers to the Intel® 82852GME GMCH
- *855GME* refers to the Intel® 82855GME GMCH
- *915GM* refers to the Intel® 82915GM GMCH
- *945GM* refers to the Intel® 82945GM GMCH
- *IEGD* refers to the Intel® Embedded Graphics Drivers and/or vBIOS
- *GMA Graphics* refers to the Intel® Graphics Media Accelerator drivers and/or vBIOS
- *Extreme Graphics* refers to the Intel® Extreme Graphics drivers and/or vBIOS

Term	Description
ANSI	American National Standards Institute http://www.ansi.org/
Bpp	Bits Per Pixel
DVO	Digital Video Out
EIA	Electronic Industries Alliance http://www.eia.org/

Term	Description
GMCH	Graphics Memory Controller Hub
LCD	Liquid Crystal Display
LFP	Local Flat Panel
LVDS	Low Voltage Differential Signaling
MMIO	Memory Mapped I/O
PSWG	Panel Standardization Working Group
RGB	Red Green Blue
SDVO	Serial Digital Video Output
SPWG	Standard Panels Working Group http://www.spwg.org/
TIA	Telecommunications Industry Association http://www.tiaonline.org/
TFT	Thin Film Transistor
TMDS	Transition Minimized Differential Signaling
UXGA	Ultra eXtended Graphics Array
vBIOS	Video BIOS
VESA	Video Electronics Standards Association http://www.vesa.org/

1.2 Reference Documents

Document	Document No./Location
Mobile Intel® 945 Express Chipset Family Datasheet	http://developer.intel.com/design/mobile/datashts/309219.htm
Mobile Intel® 945 Express Chipset Family Specification Update	http://developer.intel.com/design/mobile/specupdt/309220.htm
Mobile Intel® 915PM/GM/GMS and 910GML Express Chipset Datasheet	http://developer.intel.com/design/mobile/datashts/305264.htm
Mobile Intel® 915GM/PM/GMS and 910GML Express Chipset Specification Update	http://developer.intel.com/design/mobile/specupdt/307167.htm
Intel® 855GM/GME Chipset Graphics and Memory Controller Hub (GMCH) Datasheet	http://developer.intel.com/design/chipsets/datashts/252615.htm
Intel® 855GM/GME Chipset Graphics and Memory Controller Hub (GMCH) Specification Update	http://developer.intel.com/design/chipsets/specupdt/253572.htm
Intel(R) 855GME Chipset Graphics and Memory Controller Hub (GMCH) Specification Update Addendum	http://developer.intel.com/design/intarch/specupdt/274004.htm
Intel® 852GME Chipset GMCH and Intel® 852PM Chipset MCH Datasheet	http://developer.intel.com/design/chipsets/datashts/253027.htm
Intel® 852GME/852PM Chipset Graphics and Memory Controller Hub (GMCH) Specification Update	http://developer.intel.com/design/chipsets/specupdt/253562.htm
Intel® 852GM/852GMV Chipset Graphics and Memory Controller Hub (GMCH) Datasheet	http://developer.intel.com/design/mobile/datashts/252407.htm
Intel® 852GM/852GMV Chipset Graphics and Memory Controller Hub (GMCH) Specification Update	http://developer.intel.com/design/chipsets/specupdt/253038.htm
Intel® Embedded Graphics Driver	http://developer.intel.com/design/intarch/swsup/graphics_drivers.htm
Intel® Extreme Graphics 2	http://www.intel.com/products/chipsets/eg2/
Intel® Graphics Media Accelerator 900	http://www.intel.com/design/graphics/gma900/
Intel® Graphics Media Accelerator 950	http://www.intel.com/products/chipsets/gma950/
Embedded Intel® Architecture Software	http://developer.intel.com/design/intarch/software/index.htm

Document	Document No./Location
Binary Modification Program (BMP) Utility and User's Guide	Contact your FAE for latest revision

2 LVDS Interface Specification

This Chapter will give an overview of the LVDS interface, the difference between an 18-bpp and 24-bpp interface and how the Intel GMCHs implement the interface.

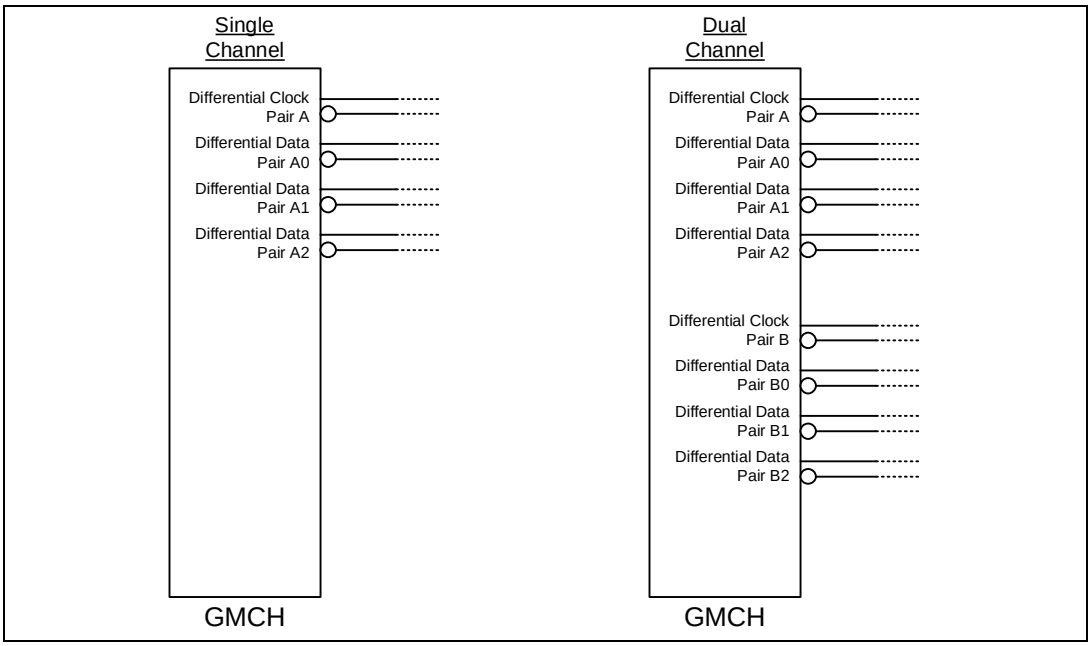
2.1 Interface Overview

The Mobile GMCH has a dedicated ANSI/TIA/EIA –644-1995 Specification compliant dual channel LFP LVDS interface that can support TFT panel resolutions up to UXGA with a maximum pixel format of 18-bpp.

Both single channel and dual channel modes are available to allow interfacing to either single or dual channel panel interfaces. This LVDS port can operate in single channel or dual channel mode. Dual channel mode uses twice the number of LVDS pairs and transfers the pixel data at twice the rate of the single channel. In general, one channel will be used for even pixels and the other for odd pixel data. The first pixel of the line is determined by the display enable going active and that pixel will be sent out channel A. All horizontal timings for active, sync, and blank will be limited to be on two pixel boundaries in the two channel modes.

A single LVDS channel and dual LVDS channel will consist of the signals indicated in Figure 1.

Figure 1: 18-bpp Single and Dual Channel LVDS Interface Signals

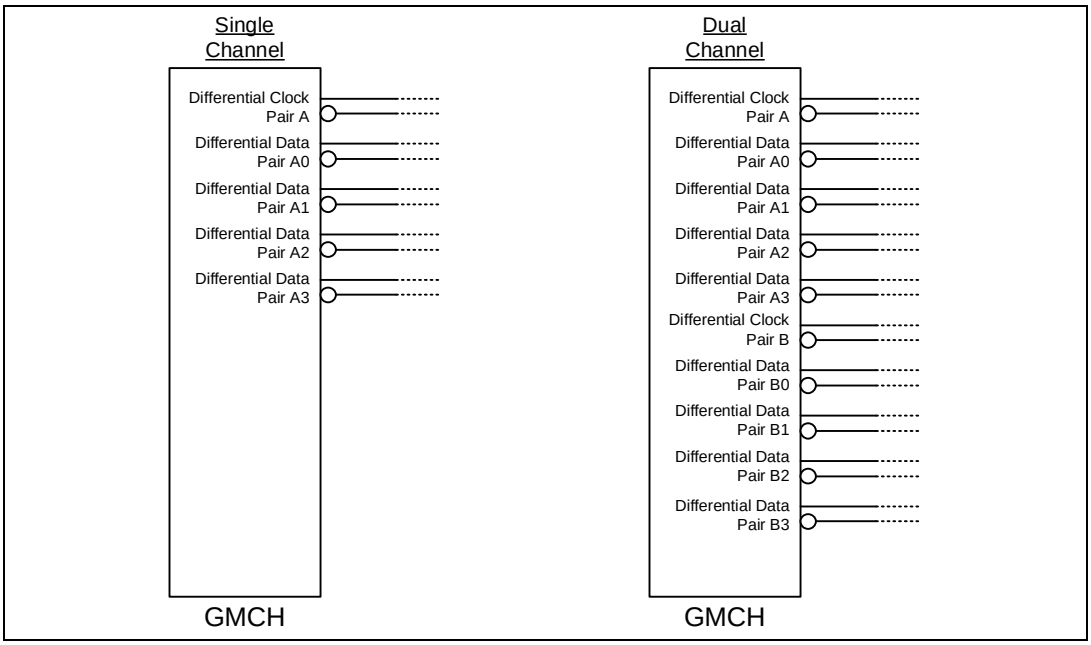


2.2 18-bpp vs 24-bpp Operation

Depending on configuration and mode, a single channel can take 18 bits of RGB pixel data plus 3 bits of timing control and output them on three differential data pair outputs; or 24 bits of RGB plus 3 bits of timing control output on four differential data pair outputs. A dual channel interface converts 36 bits or 48 bits of color information plus the 3 bits of timing control and outputs it on six or eight sets of differential data outputs.

A single LVDS channel and dual LVDS channel will consist of the signals indicated in Figure 2.

Figure 2: 24-bpp Single and Dual Channel LVDS Interfaces



3 Workarounds for using 24-bpp LVDS Panels

As stated in the Introduction, there is a growing demand from Embedded system designs to be able to use 24-bpp LVDS panels with the Mobile GMCH. This chapter details two workarounds that will allow customers to use such panels

The first workaround examines the use of an external LVDS transmitter which is connected to the GMCH via one of the SDVO interfaces. The second workaround examines how a 24-bpp panel may be connected to an 18-bpp interface while still providing a usable display output.

3.1 External LVDS Transmitter

Third party vendors have created LVDS transmitters that can be connected to the DVO or SDVO interfaces of the Mobile GMCHs. These transmitters are capable of supporting 24-bpp panels.

Chapter 3.1.1 describes the options available to Mobile GMCHs that has a DVO interface. Chapter 3.1.2 describes the options available to Mobile GMCHs that have a DVO interface.

3.1.1 DVO Transmitters

The 852GM, 852GME and 855GME Mobile GMCHs all have DVO ports for connecting to external transmitters. Figure 3 illustrates a typical connection between a Mobile GMCH and a LVDS transmitter. The transmitter must be supported in the vBIOS/driver in order to work.

Table 1 indicates which transmitters are supported in the Extreme and Embedded graphics drivers.

Figure 3: Connection of Signals Between Mobile GMCH, External LVDS Transmitter and LVDS Panel

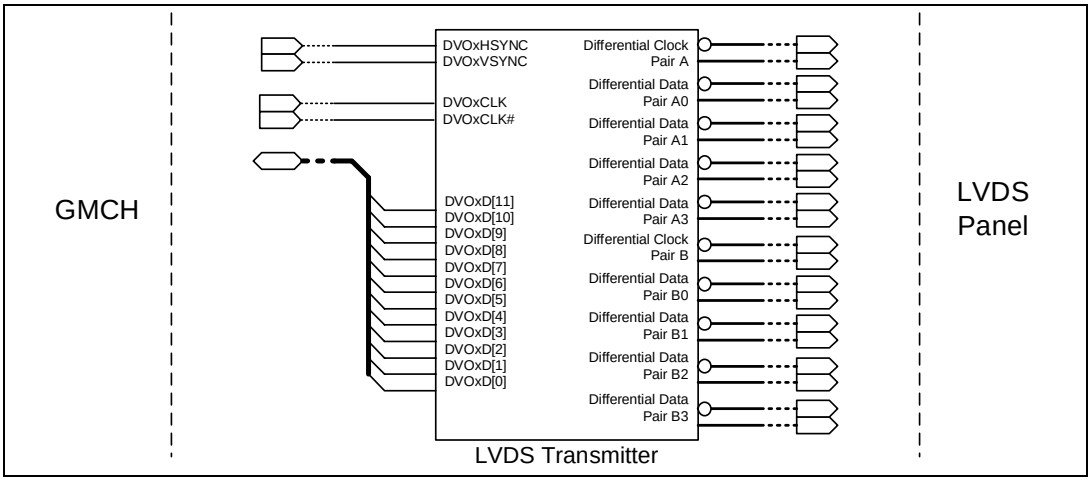


Table 1: Supported External LVDS Transmitters

Graphics Driver & vBIOS Package	Supported Transmitter
Extreme	• Chrontel*: CH7017, CH7019 • National Semiconductor*: DS90C387R, DS90C2501
Embedded	• Chrontel*: CH7017, CH7305 • National Semiconductor*: DS90C387R, DS90C2501

3.1.2 SDVO Transmitters

The 915GM and 945GM Mobile GMCHs all have SDVO ports for connecting to external transmitters. Figure 4 illustrates a typical connection between a Mobile GMCH and a LVDS transmitter. The transmitter must be supported in the vBIOS/driver in order to work. Table 2 indicates which transmitters are supported in the GMA and Embedded graphics drivers.

Figure 4: Connection of Signals Between Mobile GMCH, External LVDS Transmitter and LVDS Panel

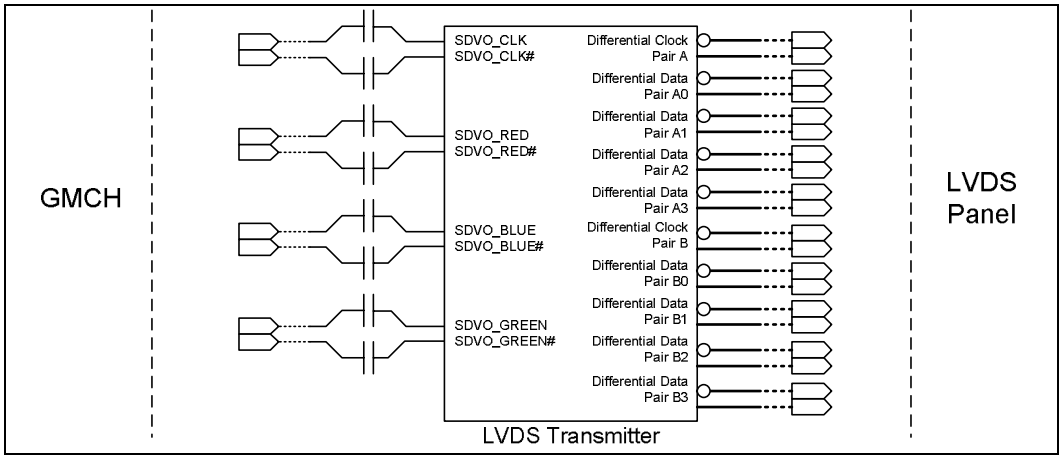


Table 2: Supported External LVDS Transmitters

Graphics Driver & vBIOS Package	Supported Transmitter
GMA	• No supported transmitter list. The vBIOS/driver uses a universal module which lists what features are enabled. Any encoder supporting those features should be enabled at the appropriate time.
Embedded	• Chrontel*: CH7308

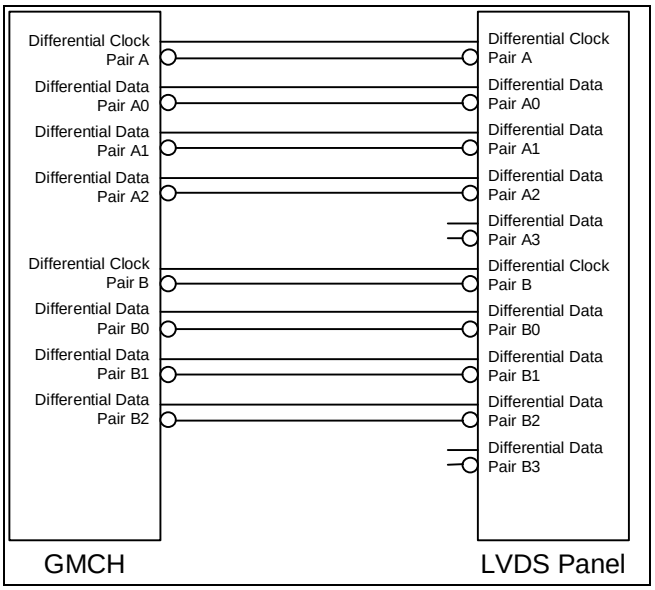
3.2 24-bpp Panel On A 18-bpp Interface

It is possible for certain types of 24-bpp panels to be connected to the integrated 18-bpp interface and still produce a usable display.

In order for a 24-bpp panel to function properly on an 18-bpp interface the panel must expect the RGB Least Significant Bits (Red[1:0], Green[1:0] and Blue[1:0]) to be transmitted on the Differential Data Pair 3. This is referred to as the 24.0 LVDS data format. Chapters 3.2.1 and 3.2.2 illustrate the differences between the 24.0 and 24.1 LVDS data formats. A panel using 24.1 LVDS data format will not work correctly when used in this configuration.

The connection between the Mobile GMCH, with an 18-bpp LVDS interface, and a 24-bpp LVDS panel is illustrated in Figure 5.

Figure 5: Connection Between An 18-bpp LVDS Transmitter and a 24-bpp LVDS Panel



The full 24-bpp range will not be available because the Differential Data Pair 3 is not being driven by the Mobile GMCH. Instead the panel is effectively operating as an 18-bpp unit.

In this configuration it is important that Bit 3 of the Panel Fitting Controls register is set to 1 even though a 24-bpp panel is being used. The Panel Fitting Controls register is described in the BMP User's Guide.

3.2.1 24.0 LVDS Data Format

Table 3: 1x24.0 (Single Channel 24-bpp)

	1	2	3	4	5	6	7
CLKA	1	1	0	0	0	1	1
A0	G<2>	R<7>	R<6>	R<5>	R<4>	R<3>	R<2>
A1	B<3>	B<2>	G<7>	G<6>	G<5>	G<4>	G<3>
A2	DE	VSYNC	HSYNC	B<7>	B<6>	B<5>	B<4>
A3	0/B<1>	B<1>	B<0>	G<1>	G<0>	R<1>	R<0>
CLKB	Off/NC						
B0	Off/NC						
B1	Off/NC						
B2	Off/NC						
B3	Off/NC						

Table 4: 2x24.0 (Dual Channel 24-bpp)

	1	2	3	4	5	6	7
CLKA	1	1	0	0	0	1	1
A0	G<2>	R<7>	R<6>	R<5>	R<4>	R<3>	R<2>
A1	B<3>	B<2>	G<7>	G<6>	G<5>	G<4>	G<3>
A2	DE	VSYNC	HSYNC	B<7>	B<6>	B<5>	B<4>
A3	0/B<1>	B<1>	B<0>	G<1>	G<0>	R<1>	R<0>
CLKB	1	1	0	0	0	1	1
B0	g<2>	r<7>	r<6>	r<5>	r<4>	r<3>	r<2>
B1	b<3>	b<2>	g<7>	g<6>	g<5>	g<4>	g<3>
B2	0/DE	0/VS/LF	0/HS/LE	b<7>	b<6>	b<5>	b<4>
B3	0/b<1>	b<1>	b<0>	g<1>	g<0>	r<1>	r<0>

3.2.2 24.1 LVDS Data Format

Table 5: 1x24.1 (Single Channel 24-bpp)

	1	2	3	4	5	6	7
CLKA	1	1	0	0	0	1	1
A0	G<0>	R<5>	R<4>	R<3>	R<2>	R<1>	R<0>
A1	B<1>	B<0>	G<5>	G<4>	G<3>	G<2>	G<1>
A2	DE	VSYNC	HSYNC	B<5>	B<4>	B<3>	B<2>
A3	0/B<7>	B<7>	B<6>	G<7>	G<6>	R<7>	R<6>
CLKB	Off/NC						
B0	Off/NC						
B1	Off/NC						
B2	Off/NC						
B3	Off/NC						

Table 6: 2x24.1 (Dual Channel 24-bpp)

	1	2	3	4	5	6	7
CLKA	1	1	0	0	0	1	1
A0	G<0>	R<5>	R<4>	R<3>	R<2>	R<1>	R<0>
A1	B<1>	B<0>	G<5>	G<4>	G<3>	G<2>	G<1>
A2	DE	VSYNC	HSYNC	B<5>	B<4>	B<3>	B<2>
A3	0/B<7>	B<7>	B<6>	G<7>	G<6>	R<7>	R<6>
CLKB	1	1	0	0	0	1	1
B0	g<0>	r<5>	r<4>	r<3>	r<2>	r<1>	r<0>
B1	b<1>	b<0>	g<5>	g<4>	g<3>	g<2>	g<1>
B2	0/DE	0/VS/LF	0/HS/LE	b<5>	b<4>	b<3>	b<2>
B3	0/b<7>	b<7>	b<6>	g<7>	g<6>	r<7>	r<6>

4 Standards of a 24-bpp Integrated LVDS Interface

The majority of LVDS Panel standards available on the market are from VESA* and SPWG. At the time of this document's publication, VESA* has proposed a draft for the 24-bpp LVDS signaling and interface connector but SPWG has submitted no standards so far. The VESA* 24-bpp standard for notebook panels is not yet widely adopted however VESA's SPWG standards for 24-bpp panels for desktop use are have already been adopted and are in wide use.

4.1 VESA* Standard Panel, 19-inch, 5-volt

Table 7 is the 30-pin assignments of 24-bpp LVDS connector that defined by VESA*. This standard has been widely adopted and accepted in the industry. Many LCD manufacturers also adopted this standard in their LCD modules. For example, Samsung* uses the VESA* 24-bpp dual channel LVDS connector in many of their monitor products. But these manufacturers have also done some changes on the sequences of the pin assignments to meet their own design goals.

Figure 6 illustrates the electrical connection between a Mobile GMCH and the 30-pin LVDS connector. Figure 7 illustrates the data format for this standard.

Table 7. 24-bpp LVDS Interface Dual Channel Pin Assignments (30-pin)

Pin No.	Symbol	Function
Frame	Vss	Ground
1	RXinO0-	-LVDS differential data input, Chan 0-Odd
2	RXinO0+	+LVDS differential data input, Chan 0-Odd
3	RXinO1-	-LVDS differential data input, Chan 1-Odd
4	RXinO1+	+LVDS differential data input, Chan 1-Odd
5	RXinO2-	-LVDS differential data input, Chan 2-Odd
6	RXinO2+	+LVDS differential data input, Chan 2-Odd
7	Vss	Ground
8	RXOC-	-LVDS differential clock input (Odd)
9	RXOC+	+LVDS differential clock input (Odd)
10	RXinO3-	-LVDS differential data input, Chan 3-Odd

Pin No.	Symbol	Function
11	RXinO3+	+LVDS differential data input, Chan 3-Odd
12	RXinE0-	-LVDS differential data input, Chan 0-Even
13	RXinE0+	+LVDS differential data input, Chan 0-Even
14	Vss	Ground
15	RXinE1-	-LVDS differential data input, Chan 1-Even
16	RXinE1+	+LVDS differential data input, Chan 1-Even
17	Vss	Ground
18	RXinE2-	-LVDS differential data input, Chan 2-Even
19	RXinE2+	+LVDS differential data input, Chan 2-Even
20	RXinEC-	-LVDS differential clock input (Even)
21	RXinEC+	+LVDS differential clock input (Even)
22	RXinE3-	-LVDS differential data input, Chan 3-Even
23	RXinE3+	+LVDS differential data input, Chan 3-Even
24	Vss	Ground
25	Vss	Ground
26	NC	No Connection
27	Vss	Ground
28	Vcc	+5.0V power supply
29	Vcc	+5.0V power supply
30	Vcc	+5.0V power supply
Frame	Vss	Ground

Figure 6. 30-pin LVDS Connector

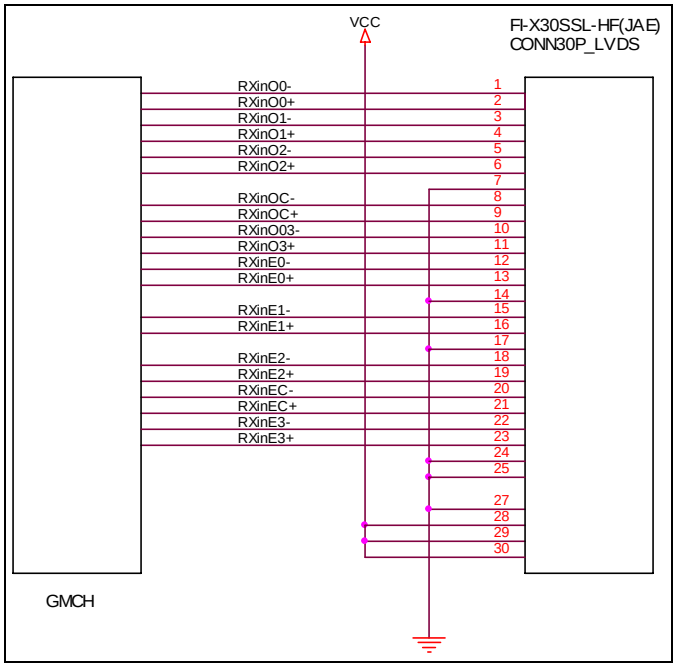
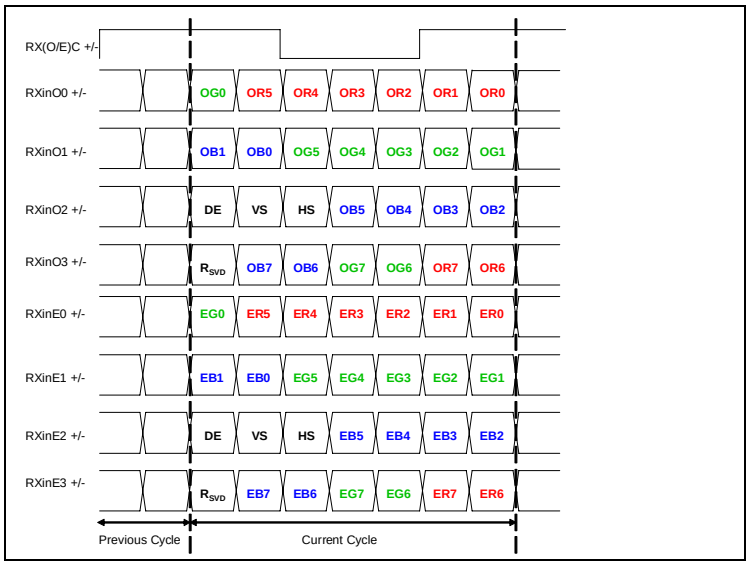


Figure 7. Dual LVDS Channel 8-bit Color Mapping for VESA* Standard Panel, 19-inch, 5-volt



4.2 PSWG* Industry Standard Panels-17.0 inch LVDS

The PSWG* Industry Standard Panels were originally created for the application as notebook panels. However, due to a lack of reference on 24-bpp integrated LVDS, some manufacturers adapted this standard for use in monitor applications. This standard established common panels for the 17.0-inch display size so that a Standard Panel can be mounted in any monitor case designed to accept the maximum size Standard Panel defined. The Standard Panel dimensions allows panel suppliers some product differentiation while meeting the goal of transparent usage across different platforms. A 24-bpp LVDS interfaced panel is defined in this standard.

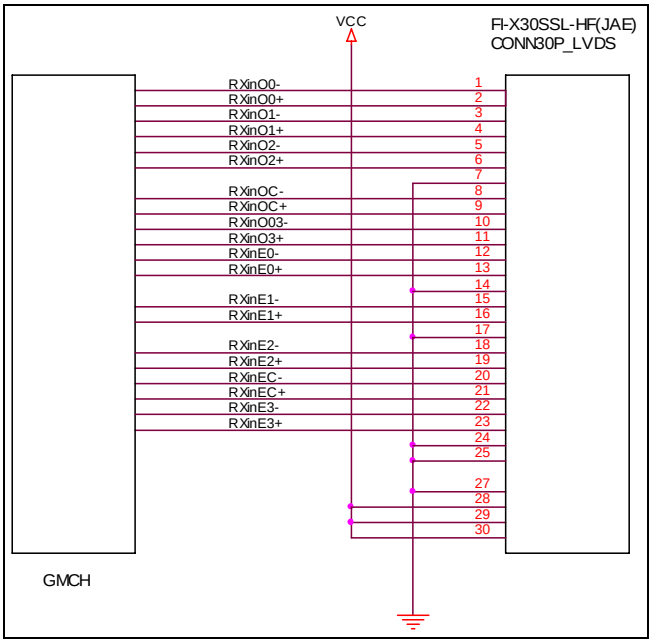
The signal interface connector for the standard is illustrated in Figure 8. The connector keep out-area shall be designed to support insertion of either a wire-crimp style connector or a wider flex-cable style connector. The interface connector pin assignments are listed in Table 8. Figure 9 illustrates the data format for this standard.

Table 8. 24-bpp LVDS Interface Dual Channel Pin Assignments

Pin No.	Symbol	Function
Frame	Vss	Ground
1	RXinO0-	-LVDS differential data input, Chan 0-Odd
2	RXinO0+	+LVDS differential data input, Chan 0-Odd
3	RXinO1-	-LVDS differential data input, Chan 1-Odd
4	RXinO1+	+LVDS differential data input, Chan 1-Odd
5	RXinO2-	-LVDS differential data input, Chan 2-Odd
6	RXinO2+	+LVDS differential data input, Chan 2-Odd
7	Vss	Ground
8	RXOC-	-LVDS differential clock input (Odd)
9	RXOC+	+LVDS differential clock input (Odd)
10	RXinO3-	-LVDS differential data input, Chan 3-Odd
11	RXinO3+	+LVDS differential data input, Chan 3-Odd
12	RXinE0-	-LVDS differential data input, Chan 0-Even
13	RXinE0+	+LVDS differential data input, Chan 0-Even
14	Vss	Ground
15	RXinE1-	-LVDS differential data input, Chan 1-Even
16	RXinE1+	+LVDS differential data input, Chan 1-Even
17	Vss	Ground
18	RXinE2-	-LVDS differential data input, Chan 2-Even
19	RXinE2+	+LVDS differential data input, Chan 2-Even

Pin No.	Symbol	Function
20	RXinEC-	-LVDS differential clock input (Even)
21	RXinEC+	+LVDS differential clock input (Even)
22	RXinE3-	-LVDS differential data input, Chan 3-Even
23	RXinE3+	+LVDS differential data input, Chan 3-Even
24	Vss	Ground
25	Vss	Ground
26	NC	No Connection
27	Vss	Ground
28	Vcc	+5.0V power supply
29	Vcc	+5.0V power supply
30	Vcc	+5.0V power supply
Frame	Vss	Ground

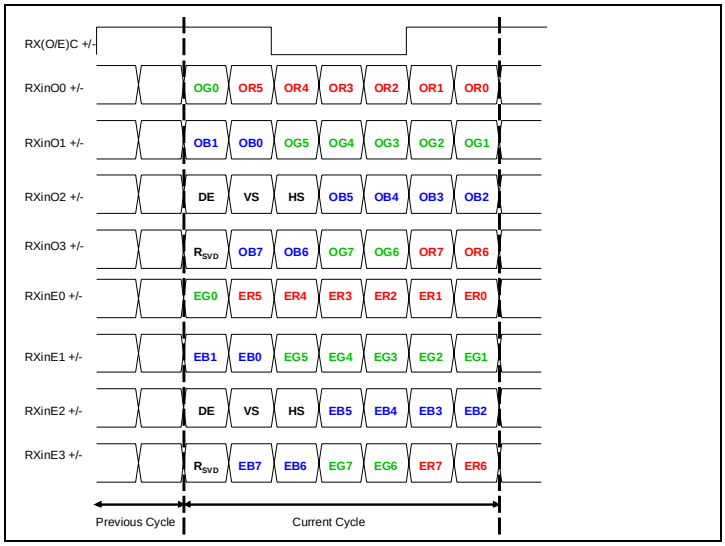
Figure 8. PSWG* Industry Standard Panel 17-inch LVDS Connector



There are some specific issues with the way mapping 24-bpp symbol encoding vs much wider 18-bpp symbol encoding. So the pin assignments in Table 8 can be also used for 18-bpp LVDS. For 18-bpp LVDS, channels RxinE3+/- and RxinO3+/- are not used by leave it no connection. Beside the input signal of even and odd clock should be the same timing.

The PSWG* Industrial Standard Panel-17 inch LVDS specification is available for download from www.vesa.org. Further details such as data and control signal interface as well as their mapping, timing specification and etc. are available in the specifications.

Figure 9. Dual Channel LVDS 8-bit Color Mapping (PSWG*)



4.3 Proposal of VESA* Standard Panel – 8-bit Interface

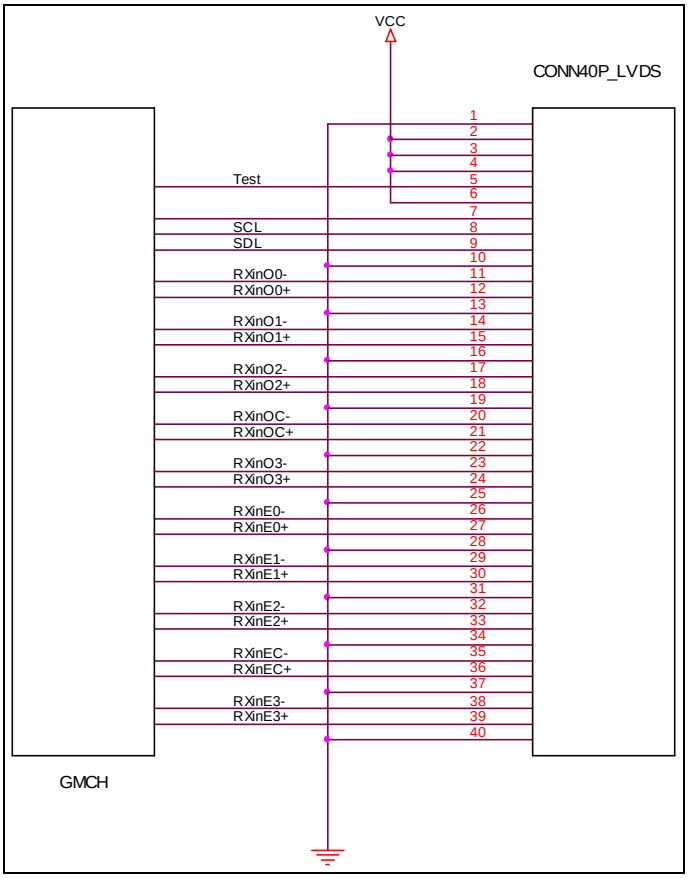
The 40-pin LVDS connector defined in Table 9 is a draft VESA* document for 24-bpp dual channel LVDS interface. This specification has not been finalized and currently still under development. Figure 10 illustrates the electrical connection between a Mobile GMCH and the 40-pin LVDS connector.

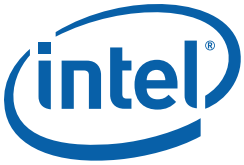
Table 9. 24-bpp LVDS Interface Dual Channel Pin Assignments (40-pin)

Pin No.	Symbol	In/Out	Function
1	Vss	G	Ground
2	D_{vDD}	P	Digital Power Supply
3	D_{vDD}	P	Digital Power Supply
4	D_{vDD}	P	Digital Power Supply
5	Test	I	Panel Test
6	V_{EEDID}	P	Digital Power Supply
7	Reserved		
8	SCL	IO	DDC clock

Pin No.	Symbol	In/Out	Function
9	SDL	IO	DDC Data
10	Vss	G	Ground
11	RXinO0-		-LVDS differential data input, Chan 0-D13
12	RXinO0+		+LVDS differential data input, Chan 0-Odd
13	Vss	G	Ground
14	RXinO1-		-LVDS differential data input, Chan 1-Odd
15	RXinO1+		+LVDS differential data input, Chan 1-Odd
16	Vss	G	Ground
17	RXinO2-		-LVDS differential data input, Chan 2-Odd
18	RXinO2+		+LVDS differential data input, Chan 2-Odd
19	Vss	G	Ground
20	RXOC-		-LVDS differential clock input (Odd)
21	RXOC+		+LVDS differential clock input (Odd)
22	Vss	G	Ground
23	RXinO3-		-LVDS differential data input, Chan 3-Odd
24	RXinO3+		+LVDS differential data input, Chan 3-Odd
25	Vss	G	Ground
26	RXinE0-		-LVDS differential data input, Chan 0-Even
27	RXinE0+		+LVDS differential data input, Chan 0-Even
28	Vss	G	Ground
29	RXinE1-		-LVDS differential data input, Chan 1-Even
30	RXinE1+		+LVDS differential data input, Chan 1-Even
31	Vss	G	Ground
32	RXinE2-		-LVDS differential data input, Chan 2-Even
33	RXinE2+		+LVDS differential data input, Chan 2-Even
34	Vss	G	Ground
35	RXinEC-		-LVDS differential clock input (Even)
36	RXinEC+		+LVDS differential clock input (Even)
37	Vss	G	Ground
38	RXinE3-		-LVDS differential data input, Chan 3-Even
39	RXinE3+		+LVDS differential data input, Chan 3-Even
40	Vss	G	Ground

Figure 10: 40-pin LVDS Connector





5 Summary

24-bpp LVDS panel support is a feature that is increasingly in demand with embedded customers. This white paper has shown the options open to a system designer to meet this demand. It has also discussed some of the standards that are associated with 24-bpp panels.